

Running Verilog-HDL
file - tutorial

LSI Design Contest 2018

The 21st

LSI 2018

Design Contest
In Okinawa

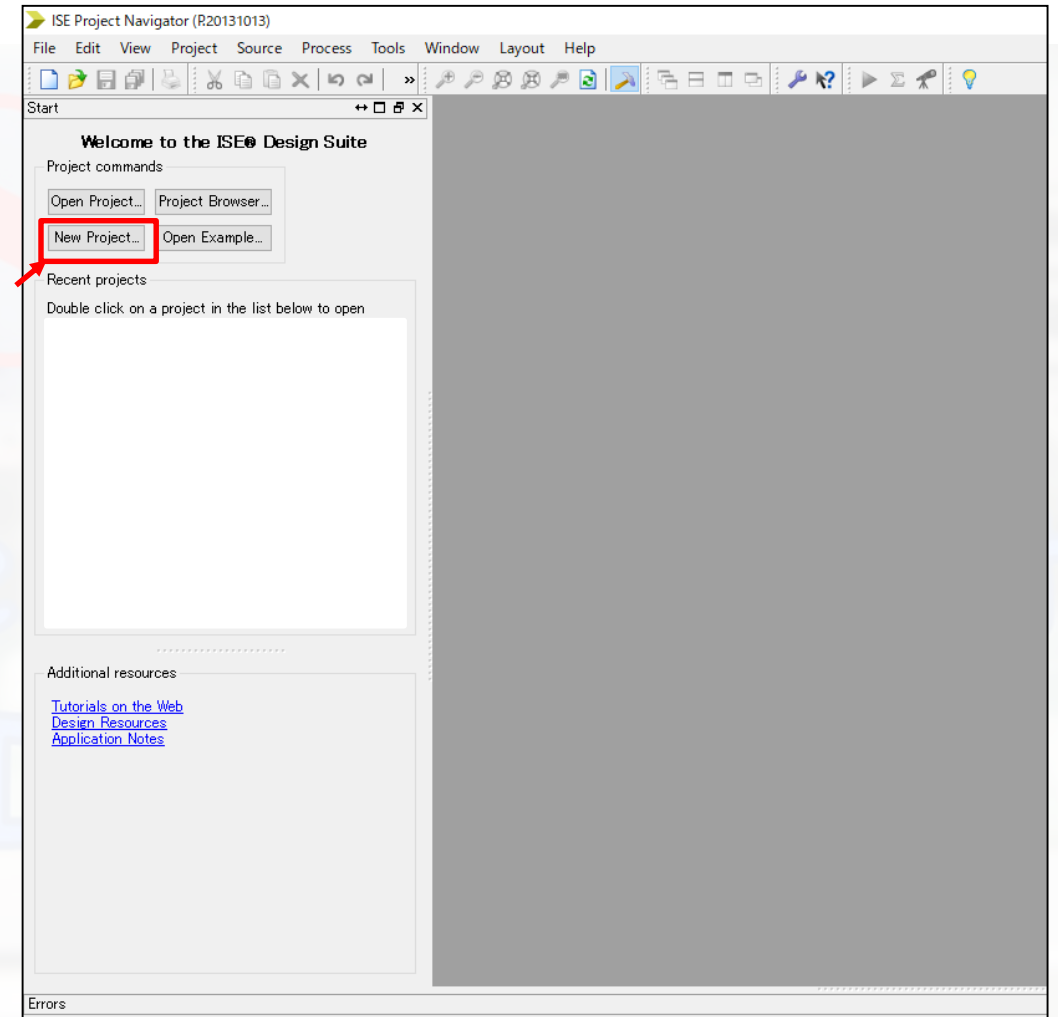
Opening ISE Design Suite

■ Open ISE Design Suite

□ Note that the version used here is 14.7



□ Next, click the 「New Project...」 as shown in the figure.



Locating project file

- Assign the location to your selected folder
- Enter the name
 - For example : NN_test
- Click, next, next and finish.

New Project Wizard

← Create New Project
Specify project location and type.

Enter a name, locations, and comment for the project

Name: NN_test

Location: D:#NN_test#NN_test

Working Directory: D:#NN_test#NN_test

Description:

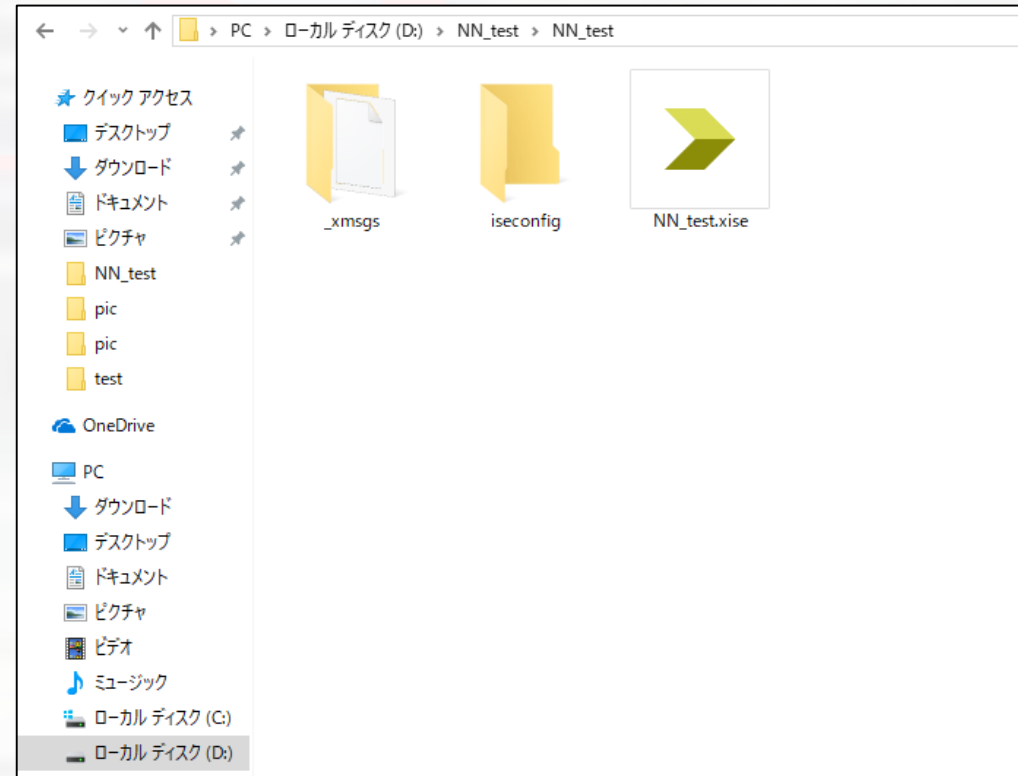
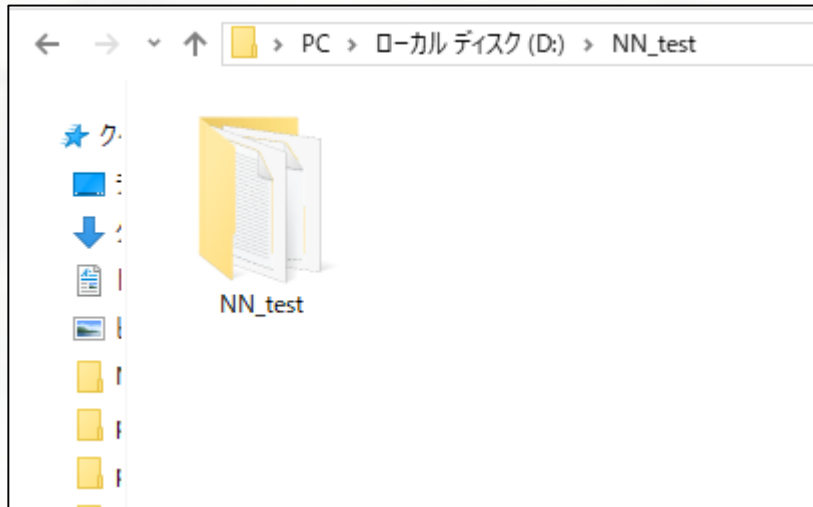
Select the type of top-level source for the project

Top-level source type:
HDL

More Info Next > Cancel

Locating project file

- A new folder will be created in your selected location



Download Verilog file

- Download the zip file from LSI design contest HP.

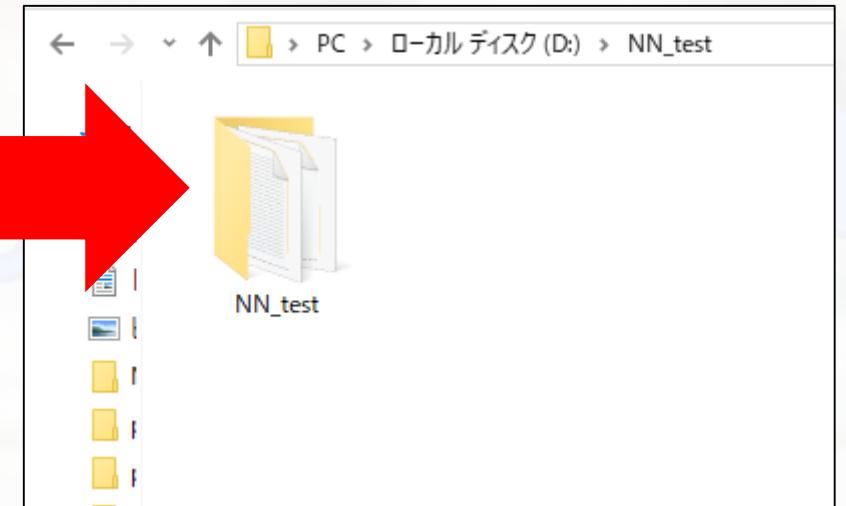
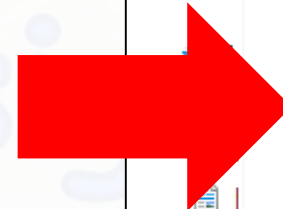
- Link : http://www.lsi-contest.com/shiyou_4e.html

- (Verilog file for simulation)

- Extract the file

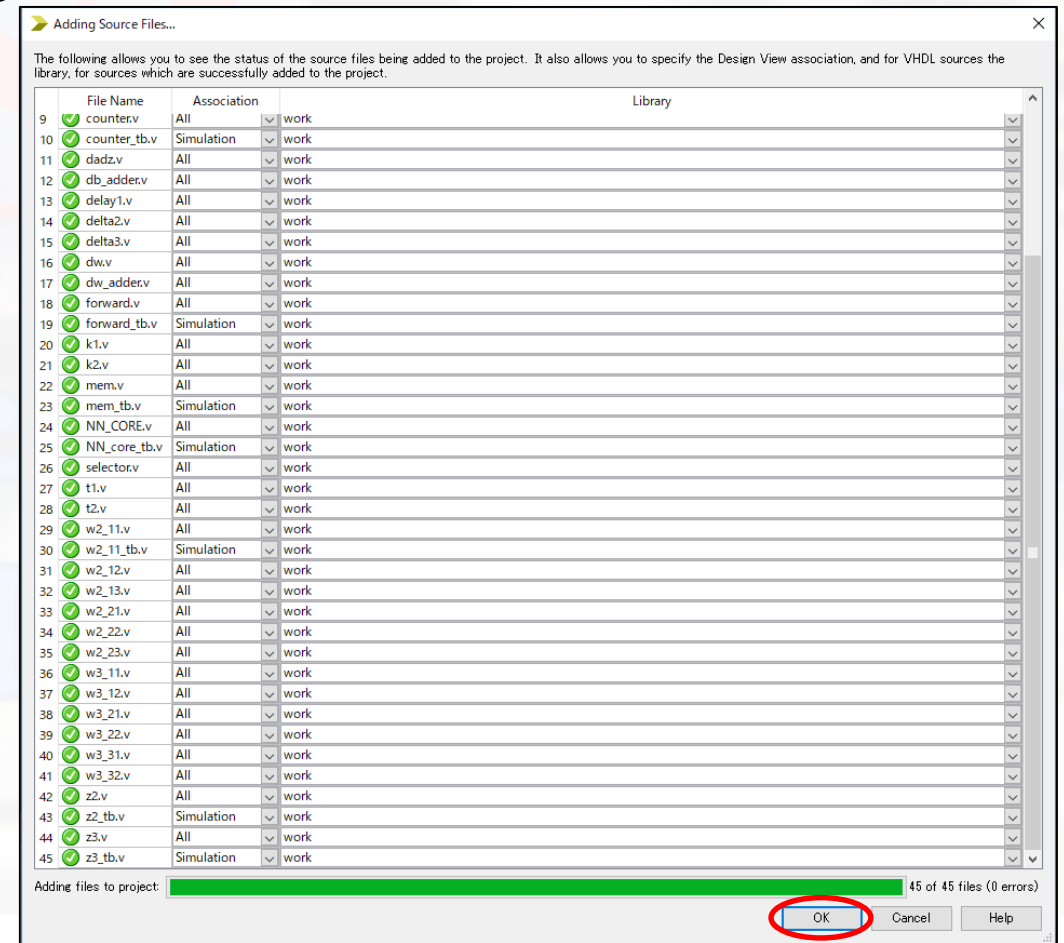
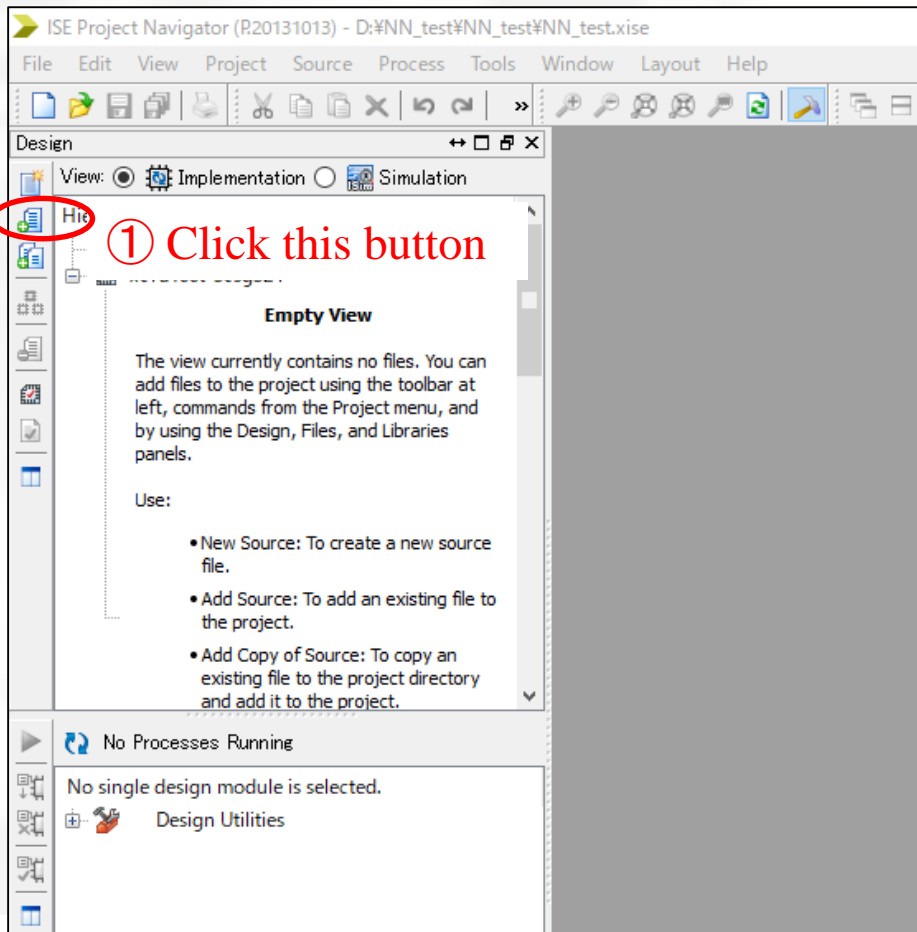
- There will be around 45 Verilog file

- Move all the Verilog file into NN_test folder



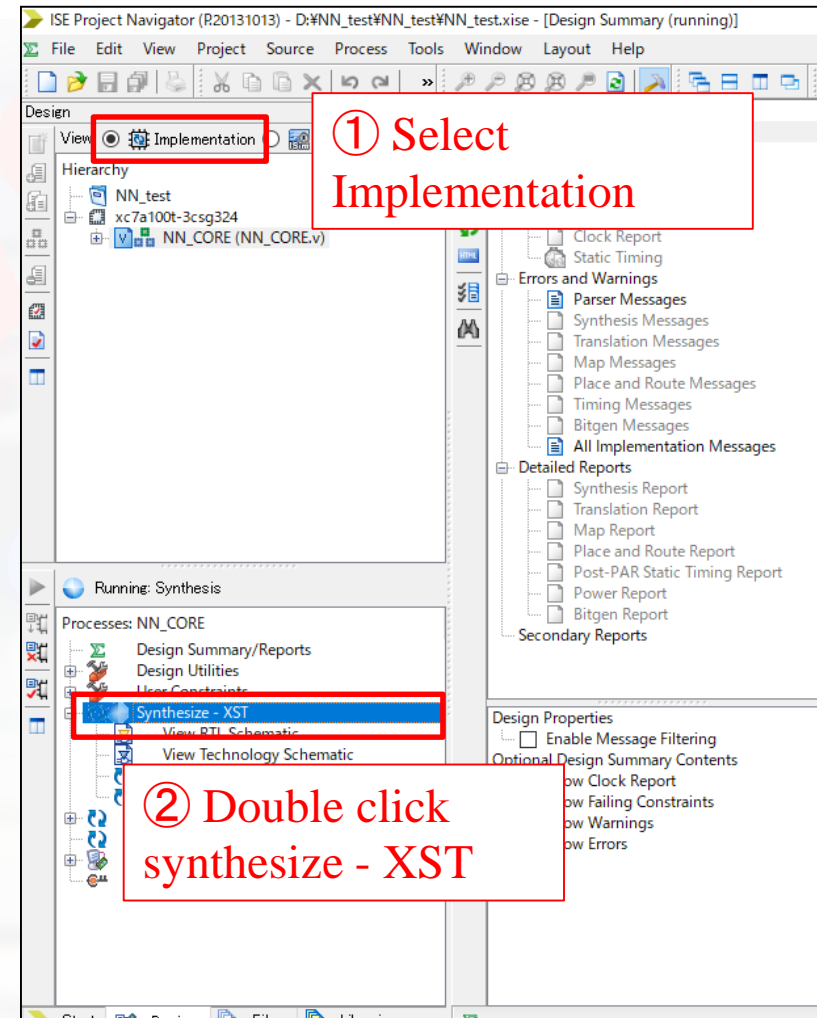
Add source file

- Click Add source and select all the Verilog file



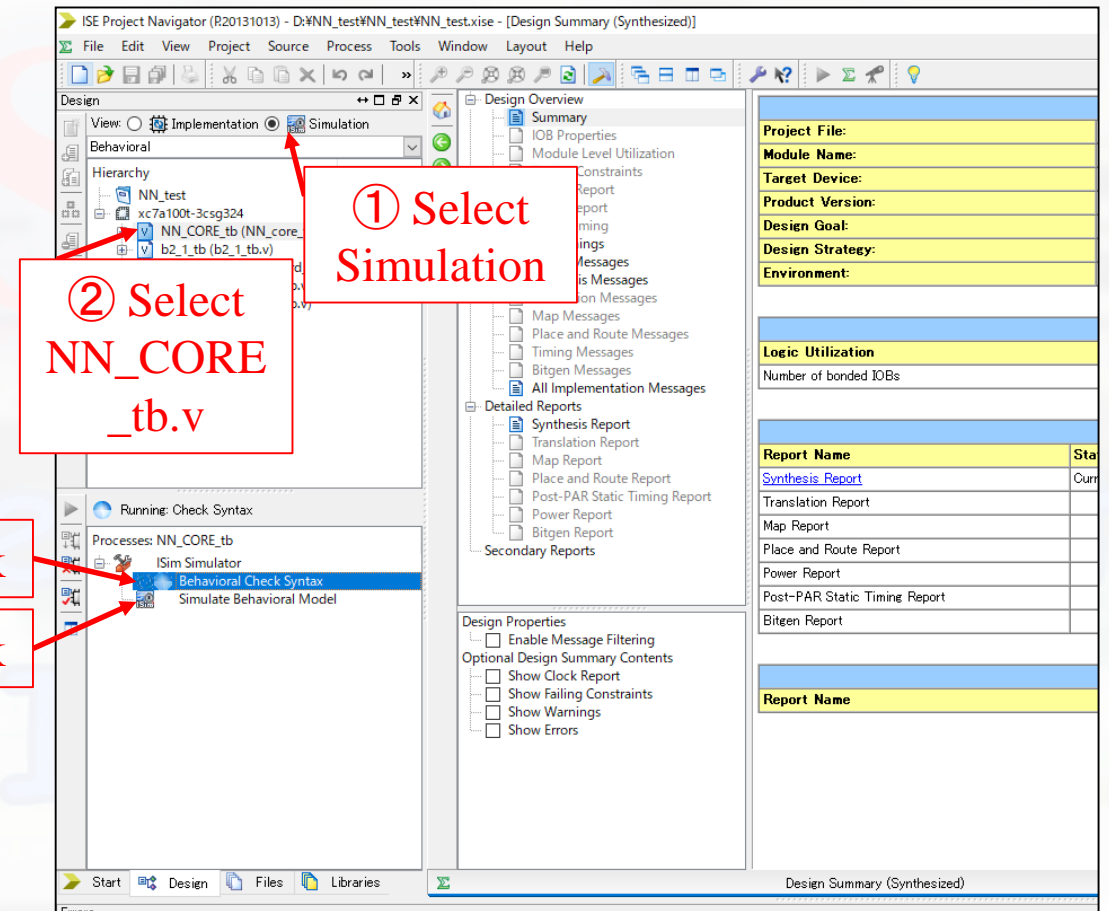
Synthesize the project

- Select Implementation
- Double click synthesize – XST
 - Wait until it finish



Simulate the project

- Select Simulation
- Double Behavioral Check Syntax
 - Wait until it finish
- Double click Simulate Behavioral Model





ISE Simulator

- ISE simulator will open
- Choose forward block in instance and process name
 - Choose signal b2_1 until w3_32
 - Drag the signal into simulator
- Choose forward > selector block in instance and process name
 - Choose signal enable update
 - Drag the signal into simulator
- See the figure in the next slide...

ISE Simulator

① open forward block

② drag this signal into simulator

Name	Value
b2_3[31:0]	11111110111011011111
b3_1[31:0]	11111110101010000110001
b3_2[31:0]	1111111000101101011010
w2_11[31:0]	1111111111010001101110
w2_12[31:0]	00000000010100001001001
w2_13[31:0]	000000000100000011001101
w2_21[31:0]	00000000001110010010000
w2_22[31:0]	000000000100000111000110
w3_12[31:0]	0000000000111011011100
w3_21[31:0]	1111111111011100111010
w3_22[31:0]	000000000100101010001111
w3_31[31:0]	00000000011111101110000
w3_32[31:0]	0000000001001010101110111
clk	0
res	0
din	1
select_initial	0
enable_update	0
STEP[31:0]	000000000000000000000000

ISE Simulator

■ Click the restart button

The screenshot displays the ISE Simulator interface. The top toolbar contains various simulation control icons. A red circle highlights the restart button, which is represented by a blue square with a white circular arrow. A red callout box with the text "① click restart button" points to this button. The main window shows a project named "ISim (R20131013) - [Default.wcfg*]" with a hierarchy of simulation objects on the left, including "NN_CORE_tb" and " uut". The central pane shows a list of simulation objects with their values, such as "renewal_w3_1..." and "clk". The right pane shows a list of signals with their values, including "b3_1[31:0]", "w2_11[31:0]", "w2_12[31:0]", "w2_13[31:0]", "w2_21[31:0]", "w2_22[31:0]", "w2_23[31:0]", "w3_11[31:0]", "w3_12[31:0]", "w3_21[31:0]", "w3_22[31:0]", "w3_31[31:0]", "w3_32[31:0]", "clk", "res", "din", "select_initial", "enable_update", and "STEP[31:0]". The bottom status bar shows the simulation time as "X1: 0.000000 us".

ISE Simulator

Click the Run All button

The screenshot displays the ISE Simulator interface. The top menu bar includes File, Edit, View, Simulation, Window, Layout, and Help. The toolbar contains various icons, with the Run All button (a play icon) circled in red. A red callout box with the text "① click Run All button" points to this button. The main workspace is divided into several panels: "Instances and Process Name" on the left, "Objects" in the middle, and a data table on the right. The data table has columns for "Name" and "Value", listing simulation objects like "renewal_w3_1...", "clk", "res", "din", and "STEP[31:0]". Below the table is a waveform viewer showing digital signals in green and black. The status bar at the bottom indicates the current file is "Default.wcfg*" and the simulation is at "X1: 1.500000 us".



Conclusion

- New weight and bias will be updated every time the enable update signal is active.
- In the current stage, the output does not converge.